REMARKS/ARGUMENTS

In the final Office action dated November 9, 2005, claims 1 - 21 were allowed and claims 22 - 30 were rejected under 35 U.S.C. § 103. Claims 1 - 30 remain pending in this application. Reconsideration and reexamination are requested for claims 22 - 30.

Claims 22 - 30 were rejected under 35 U.S.C. §103 as being unpatentable over Cesari, U.S. Patent No. 5,844,947, in view of Beat, U.S. Patent No. 5,687,352. Claims 22 and 26 are independent.

Applicant submits that independent claims 22 and 26 are not obvious in view of the cited references for several reasons. First, Beat is non-analogous art and, as such, is not a proper reference under 35 U.S.C. §103. Second, there was no motivation in the art to modify Cesari using Beat. Third, a combination of Cesari and Beat would not teach or suggest the specific limitations of claim 22 or claim 26.

MPEP 2141.01(a) states that for a reference to be analogous prior art "the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." Here, claims 22 and 26 relate to maximum likelihood sequence estimation. In contrast, Beat is directed to a memory device. Hence, Beat is not in the field of applicant's endeavor.

Moreover, Beat is not reasonably pertinent to the particular problem with which the inventor was concerned. Beat is directed to a very specific way of eliminating verification circuits and consequential delays in a circuit that communicates over bus leads having high capacitive loading. Beat discusses at column 1, line 11 - column 2, line 9, that it is directed to control circuitry that interprets user commands and activates relevant peripheral circuits (memory circuits). These peripheral circuits are connected by a bus that "is long and heavily capacitively loaded." As a result of mismatches in the loading of individual bits of the bus, different delays are associated with each of the bits. This in turn results in the system potentially being in a "transit or parasitic state" such that "an unrelated peripheral circuit may then be accidentally activated." To avoid this problem conventional circuits use a verification technique whereby latches are used to latch the values from the bus and a comparator is used to verify the

data. However, this verification technique requires the use of additional circuitry such as latches and comparators and imparts delays resulting from waiting one or more clock cycles while the verification process (e.g., the latching and comparing) is performed. Beat proposes using Gray code to reduce the number of bits that are changing on the bus. Since fewer bits are changed at one time, the delay mismatches between bits may not cause problems. As a result, the verification circuitry may be eliminated along with the associated delays imparted by the verification circuitry as discussed above.

In contrast, claims 22 and 26 relate to maximum likelihood sequence estimation. The invention described in these claims is not directed to any problems associated with circuits that would otherwise use verification circuitry to avoid problems caused by very capacitive busses. Hence, there is no need to eliminate such verification circuitry or any associated delays. Accordingly, these claims and Beat are directed toward different problems. Applicant therefore respectfully submits that Beat is nonanalogous art.

There was no motivation in the art to modify Cesari using Beat. The Office action states that "by changing states of the binary sequence by changing only one bit on any one transition, components of the circuit are eliminated and the effective speed of the circuit is increased (column 2, lines 28 - 33). For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the method of changing transitions of Beat into the detector of Cesari." Applicant respectfully submits that there was no teaching or suggestion that the above advantages from Beat were in any way applicable to Cesari.

As discussed above the advantages of Beat are due to the elimination of verification circuits and the associated delays in a circuit that communicates over bus leads having high capacitive loading. Specifically, in Beat an advantage was realized by eliminating an undesirable signal problem caused by delays in the bus leads. Hence, Beat only teaches or suggests that Gray code may provide an advantage in circuits where reducing the number of signal lines that change value at a given time reduces problems associated with delay imparted on each of those lines and where such circuits would otherwise require the use of verification circuits that require additional circuitry and impart processing delay.

There is no suggestion that the teachings of Beat may be advantageously used in other situations, much less in computing an MLSE. Accordingly, one skilled in the art attempting to develop a system for maximum likelihood sequence estimation would not have been motivated to incorporate the teachings of Beat into Cesari.

Finally, even assuming that there was a motivation to combine Beat with Cesari (which as discussed above there is none), there is no teaching or suggestion to combine the references in a manner that provides the claimed invention. For example, there was no teaching or suggestion as to which part of an MLSE process may advantageously be modified to incorporate a Gray code. More specifically, there was no teaching or suggestion that a sequencing of states could or should be advantageously modified through use of a Gray code as claimed. In summary, there is no teaching or suggestion to combine the specific portion of Beat cited by the Examiner with the specific portions of Cesari cited by the Examiner in a manner that provides the specific structure or method of claim 22, 26 or the dependent claims.

In view of the above, Applicant respectfully submits that claims 22 and 26 are not obvious in view of the cited art. Claims 23 - 25 and 27 - 30 that depend on claim 22 or claim 26 also are patentable over the cited references for the reasons set forth above. In addition, these dependent claims are patentable over the cited references for the additional limitations that the dependent claims contain. For example, regarding claims 23 and 28 there was no teaching or suggestion that for maximum likelihood sequence estimation "state values are generated in accordance with the at least one Grey code sequence." Regarding claims 25 and 30 there was no teaching or suggestion that for maximum likelihood sequence estimation "computing supporting branch metric parameters requires only a single addition operation per branch metric parameter per state." Regarding claim 27 there was no teaching or suggestion that for maximum likelihood sequence estimation "a present state is incremented to a next state by changing only one bit in accordance with the at least one Gray code sequence."

CONCLUSION

For at least the foregoing reasons Applicant submits that all of the pending the claims are patentable over the references of record. Reexamination and reconsideration are respectfully requested.

Respectfully submitted,
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